# **16.317: Microprocessor Systems Design I** Fall 2013

### Exam 1 Solution

### 1. (20 points, 5 points per part) *Multiple choice*

For each of the multiple choice questions below, clearly indicate your response by circling or underlining the single choice you think best answers the question.

- a. If AX = 0FF0h, which of the following instructions will set CF = 1 and change AX to 0EF0h?
  - A. BTR
     AX, 8

     B. BT
     AX, 8

     C. BTC
     AX, 8

     D. BTS
     AX, 8
  - *i.* <u>*A* and C</u>
  - ii. A and D
- iii. B and C
- iv. B and D
- v. None of the above

1 (continued)

b. If AX = 1001H, which of the following choices correctly shows the results of performing the two bit scan instructions (BSF and BSR) on this register?

BSF	DX,	AX	→	ZF	=	1,	DX	=	0000h
BSR	DX,	AX	$\rightarrow$	ZF	=	1,	DX	=	000Ch
BSF	DX,	AX	$\rightarrow$	$\mathbf{ZF}$	=	1,	DX	=	0000h
BSR	DX,	AX	$\rightarrow$	$\mathbf{ZF}$	=	1,	DX	=	0003h
BSF	DX,	AX	$\rightarrow$	$\mathbf{ZF}$	=	Ο,	DX	=	0000h
BSR	DX,	AX	$\rightarrow$	$\mathbf{ZF}$	=	Ο,	DX	=	000Ch
BSF	DX,	AX	$\rightarrow$	ZF	=	1,	DX	=	000Ch
BSR	DX,	AX	$\rightarrow$	ZF	=	1,	DX	=	0000h
BSF	DX,	AX	$\rightarrow$	ZF	=	Ο,	DX	un	changed
BSR	DX,	AX	$\rightarrow$	ZF	=	Ο,	DX	un	changed
	BSF BSF BSF BSF BSF BSF	BSR DX, BSR DX, BSR DX, BSF DX, BSR DX, BSF DX, BSR DX,	BSF DX, AX BSR DX, AX BSF DX, AX BSR DX, AX BSF DX, AX BSR DX, AX BSF DX, AX BSF DX, AX BSF DX, AX BSF DX, AX	BSR DX, AX $\rightarrow$ BSF DX, AX $\rightarrow$ BSR DX, AX $\rightarrow$ BSF DX, AX $\rightarrow$	BSR DX, AX $\rightarrow$ ZFBSF DX, AX $\rightarrow$ ZF	BSR DX, AX $\rightarrow$ ZF =BSF DX, AX $\rightarrow$ ZF =BSR DX, AX $\rightarrow$ ZF =BSF DX, AX $\rightarrow$ ZF =	BSR DX, AX $\rightarrow$ ZF = 1,BSF DX, AX $\rightarrow$ ZF = 1,BSR DX, AX $\rightarrow$ ZF = 1,BSF DX, AX $\rightarrow$ ZF = 0,BSR DX, AX $\rightarrow$ ZF = 0,BSF DX, AX $\rightarrow$ ZF = 1,BSF DX, AX $\rightarrow$ ZF = 1,BSF DX, AX $\rightarrow$ ZF = 1,BSF DX, AX $\rightarrow$ ZF = 0,	BSR DX, AX $\rightarrow$ ZF = 1, DXBSF DX, AX $\rightarrow$ ZF = 1, DXBSR DX, AX $\rightarrow$ ZF = 1, DXBSR DX, AX $\rightarrow$ ZF = 1, DXBSF DX, AX $\rightarrow$ ZF = 0, DXBSF DX, AX $\rightarrow$ ZF = 0, DXBSF DX, AX $\rightarrow$ ZF = 1, DXBSF DX, AX $\rightarrow$ ZF = 1, DXBSF DX, AX $\rightarrow$ ZF = 1, DXBSF DX, AX $\rightarrow$ ZF = 0, DXBSF DX, AX $\rightarrow$ ZF = 0, DX	BSR DX, AX $\rightarrow$ ZF = 1, DX =BSF DX, AX $\rightarrow$ ZF = 1, DX =BSR DX, AX $\rightarrow$ ZF = 1, DX =BSF DX, AX $\rightarrow$ ZF = 0, DX =BSR DX, AX $\rightarrow$ ZF = 0, DX =BSF DX, AX $\rightarrow$ ZF = 1, DX =BSF DX, AX $\rightarrow$ ZF = 0, DX un

c. If AX = 000Fh and CF = 0, initially, what is the result of the instruction ROR AX, 4?

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i. AX = 00F0h, CF = 0
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# $ii. \quad \underline{AX = F000h, \ CF = 1}$

- iii. AX = E000h, CF = 1
- iv. AX = 0000h, CF = 1
- v. AX = 00FFh, CF = 1

1 (continued)

d. If AX = 0001h and CF = 1, initially, what is the result of the instruction RCL AX, 2?

- i. AX = 0000h, CF = 0
  ii. AX = 0003h, CF = 0
  iii. AX = 0004h, CF = 0 *iv.* <u>AX = 0006h, CF = 0</u>
- v. AX = 1000h, CF = 1

#### 2. (30 points) *Data transfers and memory addressing*

For each data transfer instruction shown below, list <u>all</u> changed registers and/or memory locations and their final values. If memory is changed, be sure to explicitly list <u>all changed</u> <u>bytes</u>. Also, indicate if each instruction performs an aligned memory access, an unaligned memory access, or no memory access at all.

Initial state:					
EAX: 0000000h	Address	Lo			Hi
EBX: 0000006h	93000h	B0	21	AA	36
ECX: 0000001h	93004h	15	99	FE	0C
EDX: 0000FF00h	93008h	CE	12	60	EB
ESI: 0000F000h	9300Ch	89	0A	0B	FF
EDI: 00001000h	93010h	00	11	03	20
DS: 9300h	93014h	08	17	A1	B8
ES: 9200h	93018h	99	30	CB	ED

Instructions:

ES:[DI+10h], BL <u>Aligned?</u> <u>Yes</u> No Not a memory access MOV EA = DI + 0010h = 1000h + 0010h = 1010hSBA = 92000h (access ES)LA = SBA + EA = 92000h + 1010h = 93010hByte @ 93010h = BL = 06h DI, [SI+4\*CX]Aligned? Yes No Not a memory access LEA EA = SI + (4 \* CX) = F000h + (4 \* 0001h) = F004hDI = EA = F004hAligned? Yes *No* Not a memory access MOV AX, [SI+1003h]  $EA = SI + 1003h = F000h + 1003h = \frac{1}{2}0003h$  (EA is only 16 bits) SBA = 93000h (access DS)LA = SBA + EA = 93000h + 0003h = 93003hAX = word @ 93003h = 1536h MOVZX EDX, BYTE PTR ES: [BX+1000h] Aligned? Yes No Not a memory access EA = BX + 1000h = 0006h + 1000h = 1006hSBA = 92000h (access ES)LA = SBA + EA = 92000h + 1006h = 93006hEDX = zero-extended byte @ 93006h = 000000FEh MOVSX EBX, WORD PTR [000Eh] Aligned? <u>Yes</u> No Not a memory access EA = 000EhSBA = 93000h (access DS)LA = SBA + EA = 93000h + 000Eh = 9300EhEBX = sign-extended word at 9300Eh = FFFFFF0Bh

### 3. (25 points) Arithmetic instructions

For each instruction in the sequence shown below, list <u>all</u> changed registers and/or memory locations and their new values. If memory is changed, be sure to explicitly list <u>all changed</u> <u>bytes</u>. Where appropriate, you should also list the state of the carry flag (CF).

Initial state:					
EAX: 0000FFF7h	Address	Lo			Hi
EBX: 000000A4h	31700H	04	00	08	00
ECX: 0000003h	31704H	83	00	01	01
EDX: 0000FFFEh	31708H	05	01	71	31
CF: 1	3170CH	20	40	60	80
ESI: 0000004H	31710H	02	00	AB	0F
DS: 3170H	31714H	00	16	11	55

Instructions:

SBB	BX, [SI]
	= SI = 0004H; SBA = 31700 (access DS) $\rightarrow$ LA = 31704h = BX - word at 31704h - CF = 00A4h - 0083h - 1 = $0020h$
ADD	AX, BX
	= AX + BX = FFF7h + 0020h = 0017h = 1
DEC	AX
AX	$= AX - 1 = \underline{0016h}$
IDIV	CL
	= AX / CL = 0016h / 03h = 22 / 3 = 7 = <u>07h</u> = AX % CL (remainder) = 22 % 3 = 1 = <u>01h</u>
NEG	DL
DL	$= -DL = -FEh = -(1111 \ 1110_2)$

 $= 0000 \ 0001_2 + 1 = 0000 \ 0010_2 = 02h$ 

#### 4. (25 points) *Logical instructions*

For each instruction in the sequence shown below, list <u>all</u> changed registers and/or memory locations and their new values. If memory is changed, be sure to explicitly list <u>all changed</u> <u>bytes</u>. Where appropriate, you should also list the state of the carry flag (CF).

Initial state: EAX: 000000E7h Address Hi Lo EBX: 00003300h 72300h C0 00 02 10 ECX: 0000002h 72304h 5A 10 10 15 EDX: 0000F63Ch 72308h 89 05 Β1 01 CF: 0 7230Ch 40 AC DC 20 DS: 7230h 72310h 04 08 05 83 Instructions: XOR AL, [ODH] LA = SBA + EA = 72300h + 0Dh = 7230Dh= AL XOR (byte at 7230Dh) = E7h XOR 40h = A7h AL AND AL, BH AL = AL AND BH = A7h AND 3Ch = 23hROR AL, CL AL = AL rotated right 2 bits (since CL = 2) = 23h rotated right 2 bits = 0010  $0011_2$  rot. right 2 bits  $= 1100 \ 1000_2 = C8h$ CF = copy of last bit rotated out = 1SAR AL, 4 AL = AL >> 4 (arithmetic shift)  $= C8h >> 4 = 1100 \ 1000_2 >> 4 = 1111 \ 1100_2 = FCh$ CF = last bit shifted out = 1 RCL AL, 3 AL = AL rotated left through carry 3 bits  $(CF,AL) = 1 1111 1100_2$  rotated left 3 bits  $= 1 1110 0111_{2}$  $AL = 1110 \ 0111_2 = E7h, CF = 1$ 

# 5. (10 points) *Extra credit*

Complete the program below by writing the appropriate x86 instruction into each of the blank spaces. The purpose of each instruction is described in a comment to the right of the blank.

<u>MOV AX, 6317h</u>	; Use two instructions ; to establish 63170h
	; as the starting address
MOV DS, AX	; of the data segment
<u>LES SI, [0000h]</u>	<pre>; Load the first two ; bytes stored in ; the current data ; segment into SI, ; and the next two ; bytes into ES</pre>
<u>LEA DI, [SI+1000h]</u>	<pre>; Set DI = SI + 1000h ; using a single ; instruction</pre>
MOV AX, ES:[SI]	<pre>; Load two bytes of data ; into AX from the ; extra segment (ES), ; starting at offset ; specified by SI</pre>
MOV BX, ES:[SI+2]	<pre>; Load the next two ; bytes of data from ; the extra segment ; into BX</pre>
ADD AX, BX	; Find the sum of the ; previous two values
<u>SAR AX, 1</u>	<pre>; Divide the result of ; the previous ; instruction by 2 ; without using a ; divide instruction ; Keep the sign intact</pre>
MOV ES:[DI], AX	<pre>; Store the previous ; instruction's result ; into the extra ; segment at offset ; specified by DI</pre>