16.317: Microprocessor-Based Systems I

Fall 2012

Exam 2
November 7, 2012

Name: _____ **ID #:** _____

For this exam, you may use a calculator and one 8.5" x 11" double-sided page of notes. All other electronic devices (e.g., cellular phones, laptops, PDAs) are prohibited. If you have a cellular phone, please turn it off prior to the start of the exam to avoid distracting other students.

The exam contains 3 questions for a total of 100 points. Please answer the questions in the spaces provided. If you need additional space, use the back of the page on which the question is written and clearly indicate that you have done so.

You will be provided with six pages (3 double-sided sheets) of reference material: a list of the 80386 instructions and condition codes we covered, as well as the PIC 16F684 instruction set and memory map. You do not have to submit these pages when you turn in your exam.

You will have 50 minutes to complete this exam.

Q1: Multiple choice	/ 20
Q2: Protected mode memory accesses	/ 40
Q3: Reading PIC assembly language	/ 40
TOTAL SCORE	/ 100

1. (20 points, 5 points per part) ***Multiple choice***

For each of the multiple choice questions below, clearly indicate your response by circling or underlining the single choice you think best answers the question.

a. Which of the following statements most accurately describes the role of the LDTR in 80386 protected mode?

i. The LDTR directly provides the base address and limit for the global descriptor table.

ii. The LDTR directly provides the base address and limit for the current local descriptor table.

iii. The LDTR is a selector that points to a descriptor in the global descriptor table. This descriptor directly provides the base address and limit for the current local descriptor table.

iv. The LDTR is a selector that points to a descriptor in the global descriptor table. This descriptor directly provides the base address and limit for the current data segment.

v. The LDTR is a selector that points to a descriptor in the current local descriptor table. This descriptor directly provides the base address and limit for the current data segment.

b. Say you have a high-level program containing an array of `short int` values, `X[30]`, and an integer variable, `i`. If the base address of this array is 31700000H and the value of `i` is 2, what is the address of the array element `X[i]`? Assume `short int` values hold 16 bits.

i. 31700000H

ii. 31700002H

iii. 31700004H

iv. 31700008H

1 (cont.)

c. Given the conditional statement below:

```
if (AX == BX)
   CX++;
else
   CX--;
```

Which of the following assembly sequences correctly implements this conditional statement?

i.
```
     CMP  AX, BX
     JE   L1
     DEC  CX
     JMP  L2
L1:  INC  CX
L2:                ; End of statement
```

ii.
```
     CMP  AX, BX
     JNE  L1
     DEC  CX
     JMP  L2
L1:  INC  CX
L2:                ; End of statement
```

iii.
```
     CMP  AX, BX
     JE   L1
     DEC  CX
L1:  INC  CX
L2:                ; End of statement
```

iv.
```
     CMP  AX, BX
     JNE  L1
     DEC  CX
L1:  INC  CX
L2:                ; End of statement
```

1 (cont.)

d. Which of the following pieces of information related to function calls are stored on the stack?

   A. The function's return address
   B. The starting address of the function
   C. Function arguments (i.e., values passed to the function)
   D. Local variables (i.e., variables declared inside the function)
   E. The function's name

   i. A and C
   ii. A, B, and C
   iii. A, C, and D
   iv. B, C, and D
   v. All of the above (A, B, C, D, and E)

2. (40 points) ***Protected mode memory accesses***

Assume the 80386 is running in protected mode with the state given below. Note that each memory location shown contains a descriptor for a particular segment. Also, please note that you cannot assume the memory range shown contains the entire GDT and LDT.

GDTR = 117201500050
LDTR = 0010 ***(incorrectly written as 0008 in original exam)***
LDTR cache: base = 11720128
LDTR cache: limit = 0027

DS = 0007
ES = 001F
SS = 0003
ESI = 00001202
EBP = 00000FC4

Memory	Address
Base = 030010F0 Limit = 020F	11720120
Base = 0FEE0110 Limit = 0FEC	11720128
Base = A0331010 Limit = 0027	11720130
Base = FE002200 Limit = FFFF	11720138
Base = 011B1002 Limit = 0AFF	11720140

Memory	Address
Base = AC000000 Limit = 0317	11720148
Base = 01610200 Limit = 03F7	11720150
Base = 11620128 Limit = FFFF	11720158
Base = 11720128 Limit = 0027	11720160
Base = 11720120 Limit = 0007	11720168

What physical address does each of the following instructions access?

a. `MOVSX  DX, BYTE PTR SS:[BP-4]`

b. `ADD  AX, [SI]`

c. `ROR  WORD PTR ES:[SI+10H], 7`

3. (40 points, 20 points per part) ***Reading PIC assembly language***

Show the result of each PIC 16F684 instruction in the sequences below. Be sure to show not only the state of updated registers, but also the carry (C) and zero (Z) bits.

a.
```
cblock 0x20
    x
endc
clrf    x

movlw   0x72

addlw   0xF0

movwf   x

comf    x, W

bsf     x, 4

incf    x, F

sublw   0x02

swapf   x, F

addwf   x, W
```

3 (cont.)

b.
```
    cblock 0x20
        q
    endc
    movlw   0x0B

    movwf   q

    xorlw   0x33

    iorwf   q, W

    andlw   0x87

    bsf     STATUS, C

    rlf     q, F

    btfss   q, 7

    goto    L1

    rrf     q, W

L1: andwf   q, F
```