16.317: Microprocessor-Based Systems I

Fall 2012

Exam 1
October 3, 2012

Name: _____ ID #: _____

For this exam, you may use a calculator and one 8.5" x 11" double-sided page of notes. All other electronic devices (e.g., cellular phones, laptops, PDAs) are prohibited. If you have a cellular phone, please turn it off prior to the start of the exam to avoid distracting other students.

The exam contains 3 questions for a total of 100 points. Please answer the questions in the spaces provided. If you need additional space, use the back of the page on which the question is written and clearly indicate that you have done so.

You will be provided with four pages (2 double-sided sheets) of reference material for the exam: a list of the 80386 instructions and condition codes we have covered thus far. You do not have to submit these pages when you turn in your exam.

You will have 50 minutes to complete this exam.

Q1: Multiple choice	/ 20
Q2: Memory addressing	/ 40
Q3: Assembly language	/ 40
TOTAL SCORE	/ 100

1. (20 points, 5 points per part) ***Multiple choice***
For each of the multiple choice questions below, clearly indicate your response by circling or underlining the single choice you think best answers the question.

a. Which of the following statements about data storage are **false**?

A. Registers provide fast data access because most processors have a relatively small number of registers, and those registers are located close to the part of the processor that actually performs the computation.
B. Memory locations are typically referenced by name; registers are typically referenced by address.
C. In a segmented memory architecture, the total address space is divided into fixed address ranges that cannot overlap with one another.
D. Effective address computations typically involve a constant value, one or more registers, or some combination of constants and registers.
E. The older your computer gets, the more likely it is to suffer "memory lapses"—losing its product keys, forgetting where it put data, and even failing to recognize programs it's known for years.

i. A and E

ii. B and E

iii. A, D, and E

iv. B, C, and E

v. All of the above (A, B, C, D, and E)

b. Given `AX = 0020H` and `CX = 0005H`, what is the result of the instruction: `MUL CL`?

i. `AX = 0025H`

ii. `AX = 00A0H`

iii. `AX = 0100H`

iv. `AX = 0020H`

v. `AX = 0005H`

1 (cont.)

c. Assuming A, B, C, and D are all signed integers, what compound condition does the following instruction sequence test?

```
MOV     AX, A
CMP     AX, B
SETNE   BL
MOV     AX, C
SUB     AX, A
CMP     AX, D
SETGE   BH
AND     BL, BH
```

i. `(A == B) && (C >= D)`

ii. `(A != B) && (C >= D)`

iii. `(A == B) && (C – A >= D)`

iv. `(A != B) && (C – A >= D)`

v. `(A != B) && (A – C >= D)`

d. Given the following short code sequence:

```
        MOV  CX, 10
ST:     MOV  AX, [SI]
        ADD  SI, 2
        CMP  AX, 00EFH
        LOOPNE ST
```

Under what conditions will the loop **end** (in other words, the `LOOPNE` instruction will not return to the label `ST`)?

i. `CX > 0`

ii. `(CX > 0)` and `(AX != 00EFH)`

iii. `(CX == 0)` or `(AX != 00EFH)`

iv. `(CX == 0)` or `(AX == 00EFH)`

v. `(CX == 00EFH)`

2. (40 points) ***Memory addressing***

Assume the state of the 80386DX registers are as follows:

- (CS) = 1345H
- (DS) = 3170H
- (SS) = AE01H
- (IP) = 202EH
- (ESI) = 7083F002H
- (EDI) = 102021CBH
- (EBX) = FFEE2202H
- (EBP) = 1234BEACH

Complete the table below by:

- Calculating the physical address that corresponds to each given logical address.
- Answering the alignment-related question given in the third column for each address.
    - Be sure to justify your answer in each case.

Logical address	Physical address	Alignment-related question
CS:IP		If you access a word at this address, is the access aligned? Why or why not?
SS:BP+10H		For what data sizes (byte, word, double word) will an access to this address be aligned? Why?
DS:SI+ 1002H		Say you could access 8 bytes of data (a quad word) at this address—would the access be aligned? Why or why not?
DS:BX+DI+ 101H		What is the largest amount of data that can be accessed in an aligned access to this address?

3. (40 points, 20 points per part) ***Assembly language***

For each instruction sequence shown below, list all changed registers and/or memory locations and their new values. If memory is changed, be sure to explicitly list **all changed bytes**. Where appropriate, you should also list the state of the carry flag (CF).

a. Initial state:

EAX: 00000000H
EBX: 00000008H
ECX: 0000021EH
EDX: 0000FF00H
CF: 0
ESI: 00000004H
EDI: FFFF0000H
DS: 3170H

Address	Lo			Hi
31700H	04	00	08	00
31704H	10	10	20	20
31708H	89	01	71	31
3170CH	20	40	60	80
31710H	02	00	AB	0F
31714H	00	16	11	55
31718H	17	03	7C	EE
3171CH	FF	00	42	D2
31720H	86	75	30	90

Instructions:

```
MOVSX EAX, WORD PTR [SI+0AH]


LDS   SI, [BX]


BT    BYTE PTR [00H], 2


ADC   AX, DX


NEG   AX
```

3 (cont.)
b. Initial state:

EAX: 00000038H
EBX: 00001000H
ECX: 00000004H
EDX: 0000003CH
CF: 0
ESI: 00002000H
EDI: FFFF1000H
DS: AE00H

Address	Lo			Hi
AE000H	C0	00	02	10
AE004H	10	10	15	AA
AE008H	89	01	05	B1
AE00CH	20	40	AC	DC
AE010H	04	08	05	83
AE014H	00	16	02	06
AE018H	17	03	19	78
AE01CH	FF	00	12	24
AE020H	1E	00	20	07

Instructions:

```
MOV    AL, [00H]

SAR    AL, CL

RCL    AL, 3

AND    AL, DL

BSF    BL, AL
```