16.482 / 16.561: Computer Architecture and Design

Summer 2015

Lecture 8: Key Questions
June 16, 2015

1. Describe the levels of a basic memory hierarchy.

2. Define the following: hit, miss, hit rate, miss rate

3. Define and list the formula for average memory access time (AMAT)

4. **AMAT Example:** Given the following:

   - Cache: 1 cycle access time
   - Memory: 100 cycle access time
   - Disk: 10,000 cycle access time

What is the average memory access time if the cache hit rate is 90% and the memory hit rate is 80%?

5. Explain the principle of locality, and define temporal and spatial locality.

6. Explain the basic physical organization of a cache.

7. Define the different types of block placement.

8. Example: You are given a cache with 16 lines (numbered 0-15), and a main memory module holding 2048 blocks of the same size as each cache block. Determine which cache line(s) will be used for each memory block below if the cache is (i) direct-mapped or (ii) 4-way set associative.

Block #	Cache line(s): direct-mapped	Cache line(s): 4-way set associative
0		
13		
249		

9. How are blocks identified in the cache? Show how an address can be broken down and identify the role of each field in a cache access.

10. Example: Say we have the following cache organization
    - Direct-mapped
    - 4-byte blocks
    - 32 B cache
    - 6-bit memory addresses

Given the addresses 3, 4, 6, 11, 37, and 43, answer the following questions:

a. Which addresses belong to the exact same block (i.e., both tag and index are equal)?

b. Which addresses map to the same cache line, but are part of different blocks (i.e., index numbers are equal, but tags are different?

Hint: Must convert all addresses into binary, then determine the appropriate values for each field.

11. Explain what it means for a block to be evicted from the cache. When an eviction is required in a set-associative cache, how do we choose which block to evict?

12. Describe the two different cache write policies. Which one is more commonly used, and why?

13. Example: Given the final cache and memory state shown (after walking through the first five instructions in the direct-mapped cache access example):

MEMORY:

Address		Address	
0	78	8	18
1	29	9	21
2	120	10	33
3	123	11	28
4	18	12	19
5	150	13	200
6	162	14	210
7	173	15	225

CACHE:

V	D	Tag	Data	
1	0	1	18	21
0	0	0	0	0
1	1	1	19	29
0	0	0	0	0

Determine the new cache state, as well as any modified registers and/or memory blocks, after each access listed below.

Access	Modified register	Cache state					Modified mem. block
		V	D	Tag	Data		
`lb $t1,3($zero)`							
`sb $t0,2($zero)`							
`lb $t0,11($zero)`							