16.482 / 16.561: Computer Architecture and Design

Summer 2014

Syllabus

Course Meetings

T/Th, 1-4 PM, Ball 326
F *(5/30 and 6/13 only)*, 1-4 PM, Ball 326

Course Website

Main site: http://mgeiger.eng.uml.edu/compArch/sum14

Schedule: http://mgeiger.eng.uml.edu/compArch/sum14/schedule.htm

Course Discussion Group

All course announcements will be posted on the discussion group—you are responsible for checking the board regularly or enabling direct e-mail updates from Piazza.

Sign up link: https://piazza.com/uml/summer2014/1648216561

Instructor

Dr. Michael Geiger
E-mail: Michael_Geiger@uml.edu
Office: Perry Hall 118A
Phone: 978-934-3618 (x43618 on campus)
Office hours: TTh 12-1 or by appointment

I will likely be on campus at least Tuesday, Wednesday, and Thursday during the summer term. Feel free to stop by my office, e-mail me questions, or schedule a one-on-one appointment. Office hours are subject to change.

Textbook

David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, 5th edition, 2013, ISBN: 9780124077263

Course Overview

Description: Structure of computers, past and present: first, second, third and fourth generation. Combinatorial and sequential circuits. Programmable logic arrays. Processor design: information formats, instruction formats, arithmetic operations and parallel processing. Hardwired and microprogrammed control units. Virtual, sequential and cache memories. Input-output systems, communication and bus control. Multiple CPU systems.

Credits: 3

Prerequisites: 16.265 (Logic Design) and 16.317 (Microprocessors I)

Course Overview (continued)

Course Objectives: By the end of this course, you should understand and/or be able to use all of the following:

1. **Instruction Set Architecture:** Operations and operands. MIPS instruction set.
2. **Computer Arithmetic:** Binary addition, subtraction, multiplication, and division. Floating point arithmetic.
3. **Processor Core Design:** Datapath and control design. Instruction-level parallelism. Pipelining. Multiple issue and dynamic scheduling.
4. **Memory System Design:** Principles behind memory hierarchy design. Caches. Virtual memory. Cache coherence protocols.
5. **Storage and I/O:** Disk and flash storage. I/O interfacing.
6. **Multiprocessing:** Multiprocessor systems. Multithreading. GPUs. Network topologies.

Grading: Grades will be computed on an A to F scale; A+ grades may only be assigned in the graduate course (16.561), in accordance with UMass Lowell policy. The weights assigned to the various items are:

Homework assignments	55%
Midterm exam	20%
Final exam	25%

Incomplete grades will only be given in exceptional situations, and the student must be passing the class at the time the grade is requested.

Class participation: You are responsible for all material discussed or announced in class. You are expected to attend class regularly and participate in any in-class discussions, as such exercises are essential to your learning. Although lecture attendance is not explicitly required, regular attendance will improve your understanding of the course concepts.

Exams: Make-up exams will only be offered in exceptional circumstances. You must notify Dr. Geiger as early as possible in order to determine an appropriate make-up date.

Assignment policies: Your assignments will be a mix of typical homework problems and simulation exercises that will require you to do some programming. All assignments will be posted on the course web page and discussion group.

Assignment policies include the following:

- All assignments must be completed individually unless explicitly specified.
- Late assignments are penalized at a rate of 10% per day, including weekends and holidays.
- All assignment solutions must be clearly legible.
- Although typewritten solutions are preferred, handwritten solutions are acceptable in some cases.
- All electronic submissions must be combined into a single file. If you must submit multiple files, combine them into a .zip archive—please do not use .rar format.

Academic Honesty

All assignments and exams must be completed individually unless otherwise specified. You may discuss concepts or material covered in class, but may not share any details of your solutions to assigned problems, including algorithms and code. Plagiarism (copying solutions from an outside source) is also unacceptable and will be treated as an instance of cheating.

Students are allowed to discuss assignments in general terms and to help one another fix specific errors. In this case, students are required to note that they received assistance from a classmate by listing that person's name and the nature of their assistance as part of their lab report or homework solution.

Any assignment or portion of an assignment that violates this policy will receive a grade of zero for all parties concerned. Depending on the severity of the infraction, or in cases of repeat violations, additional penalties may be given at the instructor's discretion, up to and including a failing grade in the course.

Further information on the UMass Lowell Academic Integrity Policy can be found at: http://www.uml.edu/catalog/undergraduate/policies/academic_dishonesty.htm

Acknowledgements

My sincere thanks to Jim Moran for providing me with his material from previous semesters of this course, which I used as a starting point for the development of many course materials, including this syllabus.

Course Schedule

This schedule contains a tentative schedule of topics we will cover throughout the term; the course website will contain the most up-to-date version. The web page will also describe which section(s) of the textbooks are associated with each lecture.

Please note that the exam dates are fixed—the midterm exam will be held on **Thursday, June 5**, and the final exam will be held **Thursday, June 26**.

Lecture	Date	Lecture Topics
1	T, 5/20	Course overview Computer architecture introduction Instruction set architecture
2	Th, 5/22	Digital arithmetic
3	T, 5/27	Datapath and control Pipelining
4	Th, 5/29	Instruction level parallelism Branch prediction
5	F, 5/30	Topics TBD
6	T, 6/3	Dynamic scheduling Midterm exam review
	Th, 6/5	**MIDTERM EXAM**
7	T, 6/10	Speculation
8	Th, 6/12	Multiple issue; multithreading Memory hierarchies and caching *Thursday, 6/12: Last day to withdraw (16.482)*
9	F, 6/13	Topics TBD
10	T, 6/17	More on memory hierarchies
11	Th, 6/19	Virtual memory Cache optimizations *Thursday, 6/19: Last day to withdraw (16.561)*
12	T, 6/24	Storage Multiprocessors Final Exam Review
	Th, 6/26	**FINAL EXAM**
	T, 5/20	Course overview Computer architecture introduction Instruction set architecture