

16.482 / 16.561: Computer Architecture and Design
Spring 2014

Lecture 7: Key Questions
April 3, 2014

1. Define fine-grained and coarse-grained multithreading.

2. Define simultaneous multithreading.

Multithreading example

Assume you are using a processor with the following characteristics:

- 4 functional units: 2 ALUs, 1 memory port (load/store), 1 branch
- In-order execution

Given the three threads below, show how these instructions would execute using:

- Fine-grained multithreading
- Coarse-grained multithreading
 - Switch threads on any stall over 2 cycles
- Simultaneous multithreading
 - Thread 1 is preferred, followed by Thread 2 and Thread 3

You should assume any two instructions without stalls between them are independent.

Threads:

Thread 1:

ADD.D
L.D
stall
stall
stall
stall
SUB.D
S.D
stall
BEQ

Thread 2:

SUB.D
stall
L.D
S.D
L.D
stall
ADD.D
stall
BNE

Thread 3:

L.D
stall
stall
stall
stall
stall
stall
ADD.D
stall
stall
S.D
stall
stall
BEQ

Extra space to work on multithreading example

6. **AMAT Example:** Given the following:

- Cache: 1 cycle access time
- Memory: 100 cycle access time
- Disk: 10,000 cycle access time

What is the average memory access time if the cache hit rate is 90% and the memory hit rate is 80%?

7. Explain the principle of locality, and define temporal and spatial locality.

8. Explain the basic physical organization of a cache.

9. Define the different types of block placement.

10. Example: You are given a cache with 16 lines (numbered 0-15), and a main memory module holding 2048 blocks of the same size as each cache block. Determine which cache line(s) will be used for each memory block below if the cache is (i) direct-mapped or (ii) 4-way set associative.

Block #	Cache line(s): direct-mapped	Cache line(s): 4-way set associative
0		
13		
249		