16.482 / 16.561: Computer Architecture and Design

Spring 2014

Homework #6

Due **Thursday, 4/17/14**

Notes:

- While typed submissions are preferred, handwritten submissions are acceptable.
- Any handwritten solutions that are scanned and submitted electronically must be clearly legible and combined into a single file—simply sending a picture of each scanned page is not an acceptable form of submission.

1. (50 points) You are given a system which has a 16-byte, write-back cache with 4-byte blocks. The cache is direct-mapped.

a. (10 points) If each address uses 8 bits, what size are the offset, index, and tag?

b. (40 points) Assume the initial memory state shown below for the first 16 bytes and last 16 bytes of memory (note: all addresses are listed in decimal):

Address		Address	
0	20	240	15
1	8	241	67
2	27	242	78
3	3	243	19
4	12	244	26
5	44	245	99
6	34	246	9
7	5	247	4
8	110	248	101
9	72	249	71
10	38	250	89
11	127	251	93
12	126	252	106
13	85	253	107
14	2	254	1
15	6	255	11

For each access in the sequence listed on the next page, show the cache state, indicate what register (if any) changes, and indicate if any memory blocks are written back and if so, what addresses and values are written. The cache state should carry over from one access to the next. As above, assume 8-bit addresses. Also, assume the cache is initially empty.

Instruction sequence for Question 1b:

```
lb $t0, 2($zero)
sb $t0, 0($zero)
lb $t1, 240($zero)
sb $t1, 3($zero)
lb $t0, 8($zero)
sb $t1, 248($zero)
sb $t0, 11($zero)
lb $t1, 250($zero)
lb $t3, 249($zero)
lb $t4, 243($zero)
```

2. (50 points) Repeat parts (a) and (b) of question 2, but assume a 2-way set-associative cache with the same total cache size and block size.