16.482 / 16.561: Computer Architecture and Design

Fall 2013

Lecture 3: Key Questions
September 23, 2013

1. Explain the basic hardware method for performing binary multiplication.

2. Explain the optimizations we can make to this hardware to save bits, and the operation of the refined hardware multiplier.

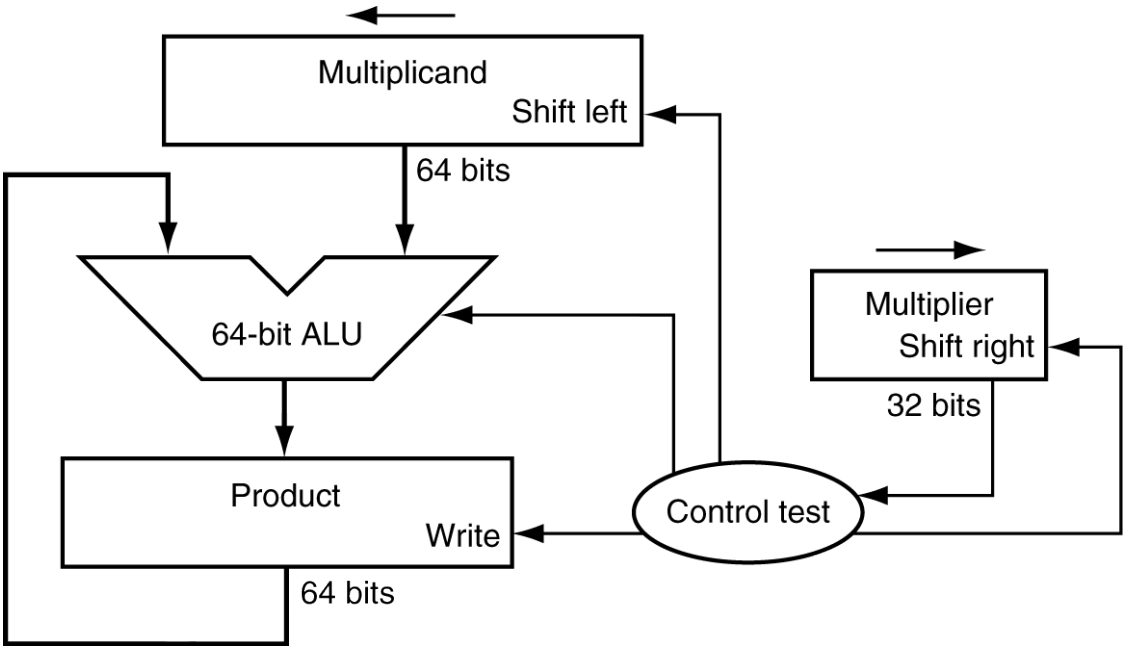

Figure 1: Basic multiplication hardware

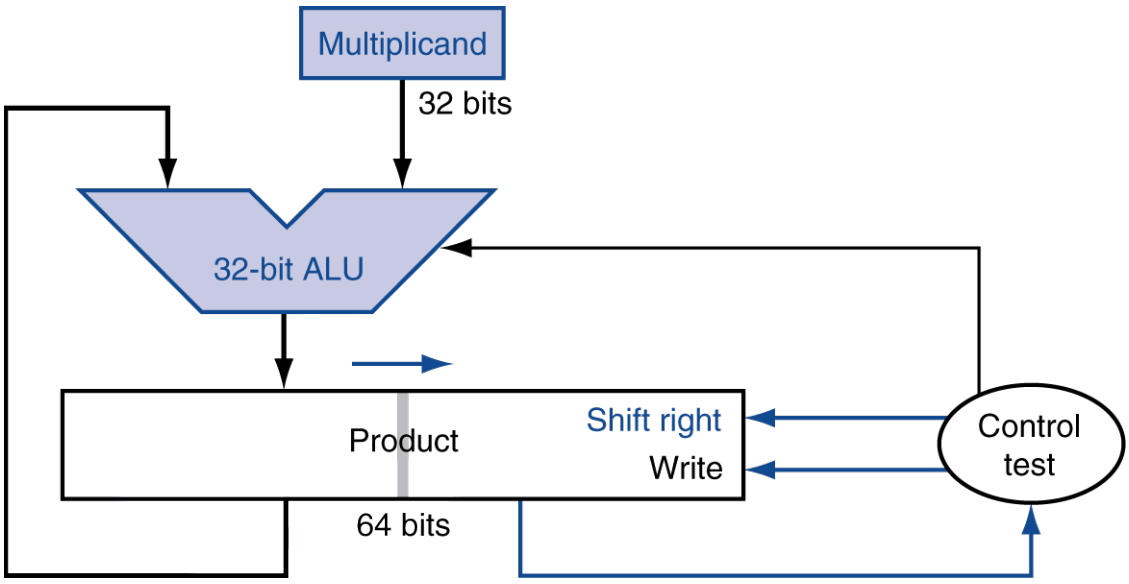

Figure 2: Optimized multiplication hardware

Show how the refined multiplier handles:

a. 4 x 3

b. 6 x 7

3. Explain the purpose and operation of Booth's Algorithm.

4. Show how Booth's Algorithm works for
a. 5 x (-3)

b. (-8) x 6

5. Explain how MIPS processors handle multiply operations.

6. Briefly describe division hardware and the MIPS divide instructions.

7. Describe the IEEE floating-point formats.

8. **Example:** Represent 0.75 in both single and double-precision floating-point format.

9. **Example:** What decimal value is represented by the single-precision float 11000000101000…00?

10. Describe floating-point addition.

11. Describe floating-point multiplication.

12. Describe the MIPS floating-point instructions.