16.482 / 16.561: Computer Architecture and Design

Fall 2013

Homework #6

Due **Monday, 11/25/13**

Notes:

- While typed submissions are preferred, handwritten submissions are acceptable.
- Any handwritten solutions that are scanned and submitted electronically <u>must</u> be clearly legible and combined into a single file—<u>simply sending a picture of each scanned page is not an acceptable form of submission</u>.

1. (30 points) For each of the following memory hierarchies, calculate the average memory access time. If you end up with a fractional number of cycles, round up—there isn't much you can do (besides read/write the register file) in half a cycle!

a. The cache takes 1 cycle to access and has a 15% miss rate, main memory takes 150 cycles to access and has an 8% miss rate, and the disk takes 30,000 cycles to access.

b. The cache takes 3 cycles to access and has a 92% hit rate, main memory takes 450 cycles to access and has a 96% hit rate, and the disk takes 15,000 cycles to access.

c. This problem deals with a multi-level cache, as discussed in class. The cache levels are listed in terms of their order in the memory hierarchy—an access initially goes to the level 1 (L1) cache. If there is a miss in the L1 cache, you then check the level 2 (L2) cache, then the level 3 (L3) cache, and then main memory.

   The L1 cache takes 1 cycle to access, with a 94% hit rate. The L2 cache takes 20 cycles on each access and has a 97% hit rate. The L3 cache takes 60 cycles to access and has a 99% hit rate. Main memory takes 500 cycles to access, with an 85% hit rate, while the disk takes 45,000 cycles to access.

2. (35 points) You are given a system which has a 16-byte, write-back cache with 4-byte blocks. The cache is direct-mapped.

a. (5 points) If each address uses 8 bits, what size are the offset, index, and tag?

b. (30 points) Assume the initial memory state shown below for the first 16 bytes and last 16 bytes of memory (note: all addresses are listed in decimal):

Address		Address	
0	20	240	15
1	8	241	67
2	27	242	78
3	3	243	19
4	12	244	26
5	44	245	99
6	34	246	9
7	5	247	4
8	110	248	101
9	72	249	71
10	38	250	89
11	127	251	93
12	126	252	106
13	85	253	107
14	2	254	1
15	6	255	11

For each access in the sequence listed below, show the cache state, indicate what register (if any) changes, and indicate if any memory blocks are written back and if so, what addresses and values are written. The cache state should carry over from one access to the next. As above, assume 10-bit addresses. Also, assume the cache is initially empty.

```
lb $t0, 2($zero)
sb $t0, 0($zero)
lb $t1, 240($zero)
sb $t1, 3($zero)
lb $t0, 8($zero)
sb $t1, 248($zero)
sb $t0, 11($zero)
lb $t1, 250($zero)
lb $t3, 249($zero)
lb $t4, 243($zero)
```

3. (35 points) Repeat parts (a) and (b) of question 2, but assume a 2-way set-associative cache with the same total cache size and block size.